CLAIMS;

Claim 1. A frequency synthesizer to lock the frequency controlled oscillator (VCO) with a reference frequency, comprising:

a reference frequency;

a phase detector;

a low pass filter to filter out any ac component from said phase detector and to derive a dc control voltage; and

a voltage controlled oscillator, whose frequency is divided by a divider to compare with said reference frequency and is controlled by said dc control voltage, which is applied in two sequential modes: a calibration mode and an analog mode,

wherein said calibration mode locks coarsely said VCO into limited number of discrete frequency steps within a predetermined frequency tolerance of the reference frequency by resetting and holding said dc control voltage in a coarse phase-locked loop, and

said analog mode starts with the said dc control voltage reset and held during the calibration mode for fine adjustment of said VCO frequency to lock with said reference frequency in a fine phase-locked loop.

Claim 2. The frequency synthesizer as described in claim 1, wherein:

said phase detector for the analog mode comprises a phase comparator and a charge pump, and

said phase detector for said calibration mode comprises a stepper to reset said dc control voltage into a predetermined number of steps and is disabled to switched to said analog mode when the dc control voltage locks the VCO frequency within a preset tolerance of said reference frequency.

Claim 3. The frequency synthesizer as described in claim2, wherein said stepper comprises a clock, a counter, and a decision-making block to incrementally step-change said dc control voltage.

Claim 4 The frequency synthesizer as described in claim 3, wherein the number of steps is a binary-weighted number.

Claim 5. The frequency synthesizer as described in claim 3, wherein said decision-making block is a control unit that selects between enabling and disabling the counter, calculates the value of the VCO dc control voltage, and selects between breaking and reconnecting the PLL for the calibration mode.

Claim 6. The frequency synthesizer as described in claim 3, wherein said counter and said decision-making block are finite state machines.